REMARKS/ARGUMENTS

Claims 1-6, 15-26, and newly added claims 31-34 are currently pending in the present patent application.

The Examiner rejected claims 1-6 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,614,748 to Nakajima *et al.* ("Nakajima") in view of U.S. Patent No. 6,800,940 B2 to Catabay *et al.* ("Catabay"). Claims 15-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakajima in view of Catabay and further in view of U.S. Patent No. 6,717,846 to Lee ("Lee").

Amended claim 1 recites a non-volatile memory cell integrated on a semiconductor substrate including a floating gate transistor including a source region and a drain region. A gate region projects from the substrate between the source and drain regions. The gate region has a predetermined length and width and includes a first floating gate region and a control gate region. The floating gate region is insulated laterally, along a direction orthogonal to a plane including the floating gate, source, and drain regions, by a dielectric layer with low dielectric constant value.

Claim 1 has been amended to recite that the dielectric layer laterally insulates the floating gate region along a direction orthogonal to a plane including the floating gate, source, and drain regions. This is illustrated, for example, in the embodiments of Figures 6 and 7. This language has been included to eliminate the Examiner's issues with the use of the term "width" direction. Thus, the floating gate regions are insulated in a direction orthogonal to the plane including the floating gate, drain and source regions. This is the direction along the word lines as discussed in our prior amendment. In other words, the dielectric layer is formed between adjacent floating gate regions for memory cells coupled to a respective word line.

Nakajima and Catabay neither disclose nor suggest the recited structure. The Examiner states that Figure 2 of Nakajima shows that insulating film 14 is formed between floating gates along a width direction, which is the direction parallel to the word lines or orthogonal to the cross-section of Figure 1 of Nakajima which is a direction parallel to the bit lines. Figure 4D of Nakajima shows a direction along a word line, or orthogonal to the plane including the floating gate, drain, and source regions. As plainly shown in Figure 4D, the floating gate 8 of memory cell pairs belonging or coupled to the same word line are coated by a polysilicon layer 12. This polysilicon layer 12 also forms the control gate of the

cells. Although not expressly shown in Figure 4D, one adjacent floating gate region would be located to the left of the floating gate region 8 shown in the figure and another adjacent floating gate region would be located to the right of the region 8. As seen from this figure, the polysilicon layer 12 completely fills the space between two adjacent floating gates regions. The floating gate regions 8 are coated by an interlayer insulating layer 10 and on top of this layer the polysilicon layer 12 is formed. The polysilicon layer 12 functions as the control gate of the memory cells and also provides electrical isolation between adjacent floating gate regions.

As the density of semiconductor devices increases, features sizes accordingly decrease. Thus, the distance between two adjacent floating gate regions belonging or coupled to the same word line decreases, for example, on the order of 40-50 nm for current state-of-the-art technologies. When the distance between adjacent floating gate regions 8 is less of the thickness of the polysilicon layer 12, it is difficult to fill the space between adjacent floating gate regions belonging or coupled to the same word line with the polysilicon layer. In this situation, voids can undesirably be formed between the adjacent floating gates. The structure recited in claim 1 is applicable in such situations since the dielectric layer can be formed to completely fill the space between two adjacent floating gate regions coupled to the same word line. See, for example, Figure 7 of the present application illustrating one embodiment of the present invention covered by claim 1 and showing the dielectric layer 9 formed between adjacent floating gates FG.

Returning now to the discussion of Nakajima, as previously mentioned the Examiner states that Figure 2 of Nakajima shows that insulating film 14 is formed between floating gates along a width direction. See page 4 of the Office Action. From the above description, this is plainly seen not to be the case. Film 14 is not even shown in Figure of Nakajima notwithstanding the Examiner's assertions. Nakajima simply does not show a dielectric layer between adjacent floating gate regions along a direction orthogonal to a plane including the floating gate, source, and drain regions. This is true, of course, except for the inter layer insulating dielectric layer 10 shown in Figure 4D, but this is precisely the structure shown in Figure 1C (layer 7) of the present application. The function of this insulating layer 10 is not to isolate adjacent floating gate regions, but instead is to isolate the floating gate and control gate regions. The layer 10 is a high dielectric constant for this purpose. In sum, Nakajima discloses the polysilicon layer 12 between adjacent floating

gate regions and neither discloses or suggests a dielectric layer between such regions. Moreover, even if dielectric layer 10 is considered a dielectric layer between adjacent floating gate regions, this layer is for an entirely different function and has nothing to do with electrically isolating adjacent floating gate regions. In fact, the region 10, being relatively high dielectric constant, could actually exacerbate coupling between adjacent floating gate regions.

Now turning to Catabay, there is no reason or suggestion to combine Catabay and Nakajima as the Examiner has done. As just explained, the dielectric layer 10 in Nakajima has a relatively high dielectric constant to provide required coupling between the control gate and floating gate regions. This is the function of this region in Nakajima. There is no disclosure or suggestion in Nakajima of using this layer 10 for electrical isolation between adjacent floating gate regions. In fact, given the purpose of the layer 10, Nakajima actually teaches away from using the low dielectric constant layer of Catabay since then the layer 10 would not be performing its required function in Nakajima. Catabay discloses the use of a low constant dielectric in order to reduce the capacitive coupling between metal lines. Thus, there is similarly no suggestion in Catabay to replace the polysilicon layer 12 in Nakajima with a low constant dielectric. In fact, the undersigned questions whether such a device could even function for it intended purpose.

Returning now the Examiner's comments regarding dielectric layer 14, which is shown in Figure 1 of Nakajima, it should be apparent from the above description that this layer is formed on top of the structure discussed above for the purpose of allowing the formation of the metal layer 16 for the bit lines. Thus, the dielectric layer 14 is not positioned between adjacent floating gate regions 8 since, as discussed with reference to Figure 4D, the polysilicon layer 12 corresponding to the control gate is in fact positioned between adjacent floating gate regions. The layer 14 is a pre-metal layer which coats the whole gate structure of the memory cells with exception of the space between adjacent floating gate regions belonging to the same word line. This is true because this space is filled by the polysilicon layer 12 as previously described.

For all these reasons, the combination of elements recited in claim 1 is allowable, and dependent claims 2-6 are allowable for at least the same reasons as claim 1. Independent claim 15, 16, and 24 are allowable for reasons similar to those set forth above

with regard to claim 1, and the associated dependent claims allowable for at least the same reasons as the corresponding independent claim.

New claim 31 recites a memory-cell structure formed on a semiconductor substrate. The memory-cell structure includes a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate. Each memory cell in a respective row is coupled to a corresponding word line and each memory cell includes a gate structure having a floating gate region and a control gate region. The memory-cell structure includes an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells coupled to a respective word line. The insulating region has a first side in direct contact with a first one of the adjacent floating gate regions and a second side in direct contact with a second one of the adjacent floating gate regions.

Neither Nakajima nor Catabay, whether taken singly or in combination, discloses an insulating region having a first side in direct contact with a first one of the adjacent floating gate regions and a second side in direct contact with a second one of the adjacent floating gate regions. There is no disclosure in Nakajima or Catabay of such an insulating regions contacting adjacent floating gate regions for cells coupled to a given word line. This structure eliminates the presence of a high dielectric constant material between adjacent floating gate regions of memory cells coupled to a respective word line. This, in turn, reduces the capacitive coupling between such floating gate regions. The high dielectric constant layer required for good capacitive coupling of the floating gate and control gate regions can then formed on top of the insulating region and floating gate regions, as recited in new claim 32. Figure 7 of the present application illustrates one embodiment of the present invention covered by these new claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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